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Signature: Shirley Fajardo

PATENT

Docket No. P1025

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS: ROBERT B. OGLE, JR.
MARK T. RAMSBY
TUAN DUC PHAM

SERIAL NO.: FILED HEREWITH

FILED: FILED HEREWITH

FOR: DUAL-PURPOSE ANTI-REFLECTIVE COATING AND SPACER
FOR FLASH MEMORY AND OTHER DUAL GATE
TECHNOLOGIES AND METHOD OF FORMING

BOX PATENT APPLICATION
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Dear Sir:

In connection with the above-referenced matter, transmitted herewith are the following:

1. Specification (5 pages), Claims (6 pages), and Abstract (1 page);
2. Formal Drawings (6 sheets);
3. Declaration and Power of Attorney for Patent Application (2 pages);
4. Assignment Agreement (3 pages);
5. Recordation Cover Sheet - Form PTO-1595 (1 page);

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Respectfully submitted,



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Signature: Shirley Fajardo

PATENT
Docket No. P1025

PATENT APPLICATION

DUAL-PURPOSE ANTI-REFLECTIVE COATING AND SPACER FOR FLASH MEMORY AND OTHER DUAL GATE TECHNOLOGIES AND METHOD OF FORMING

INVENTORS: ROBERT B. OGLE, JR.
 MARK T. RAMSBEY
 TUAN DUC PHAM

RELATED APPLICATION

This application is related to co-pending U.S. Provisional Patent Application Ser. No. 60/159,235, entitled "DUAL-PURPOSE ANTI-REFLECTIVE COATING AND SPACER FOR FLASH MEMORY AND OTHER DUAL GATE TECHNOLOGIES AND METHOD OF FORMING", filed October 13, 1999.

TECHNICAL FIELD

The present invention relates to integrated semiconductor circuits and anti-reflective coating fabrication techniques used in dual gate semiconductor technology, such as FLASH memory technology. More particularly, the present invention relates to integrated semiconductor circuits and fabrication techniques for forming sidewall structure on the sidewalls of the transistor gates used in dual gate semiconductor technology, such as FLASH memory technology. Even more particularly, the present invention relates to integrated semiconductor circuits and fabrication techniques for forming sidewall structure on the sidewalls of transistor gates in the core memory region as used in dual gate semiconductor technology, such as FLASH memory technology.

BACKGROUND OF THE INVENTION

Dual gate technology, such as FLASH memory technology, uses anti-reflective coatings to ease lithographic patterning. The closely formed dual gate transistor gates require electrical isolation provided by spacers formed on the sidewall structure of the gate stacks. Typically, a dielectric material, similar to the anti-reflective coating material, is used to form the spacers on the sidewall structure of the dual transistor gates. According to known fabrication techniques, the anti-reflective coating is used twice during formation of the spacers, which, as a result of etching and stripping action of the fabrication process, the thickness of the anti-reflective coating is reduced, resulting in a loss of the effectiveness of the anti-reflective coating. Thus, there is seen to exist a need for a fabrication technique that does not depend on deteriorated use of the anti-reflective coating to fabricate the sidewall spacers of dual gate semiconductor devices.

BRIEF SUMMARY OF THE INVENTION

Accordingly, the present invention provides a dual gate semiconductor device, such as a FLASH memory semiconductor device, whose plurality of dual gate sidewall spacer structure are not formed from traditional dielectric material similar to the anti-reflective coating material that is traditionally used for lithographic patterning. Rather, the present invention provides a dual gate semiconductor structure whose sidewall spacers are formed by a first and second anti-reflection fabrication process, whereby, the sidewall spacers of the dual transistor gate structure in the core memory region are left coated with the second anti-reflective coating material, such as silicon oxynitride (SiON), silicon nitride (Si₃N₄), and silicon germanium (SiGe), or other material having optical properties compatible with subsequent fabrication processing, to form sidewall spacers for use in subsequent implant and salicidation steps, commonly used during fabrication of the semiconductor device being formed. Other features of the present invention are disclosed or are apparent in the section entitled "DETAILED DESCRIPTION OF THE INVENTION."

BRIEF DESCRIPTION OF DRAWINGS

The invention, including its various objects, features, and advantages, may be more readily understood with reference to the following detailed description of the best mode for carrying out the invention, taken in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, as below-referenced.

5 Figure 1 is a cross-sectional view of a prior art semiconductor device shown at a fabrication stage whereby anti-reflective coating portions overlying various memory element regions will be subjected to various etching process steps after patterning.

10 Figure 2 is a cross-sectional view of a semiconductor substrate shown at a fabrication stage in accordance with the present invention where a first anti-reflective coating has been utilized for patterning core and periphery substrate regions.

Figure 3 is a cross-sectional view of the memory semiconductor substrate depicted in Figure 2 shown with the first coat of anti-reflective coating has been removed.

15 Figure 4 is a cross-sectional view of the memory semiconductor substrate depicted in Figure 3 shown at a fabrication stage where a second anti-reflective coating have been formed over the patterned core and peripheral regions in accordance with the present invention.

Figure 5 is a cross-sectional view of the memory semiconductor substrate depicted in Figure 4 shown having patterned peripheral memory regions and core memory regions fully coated with the second anti-reflective coating.

20 Figure 6 is a cross-sectional view of the memory semiconductor substrate depicted in Figure 6 shown having sidewall spacers formed from the second anti-reflective coating in accordance with the present invention.

Reference numbers refer to the same or equivalent parts of the present invention throughout the several figures of the drawings.

DETAILED DESCRIPTION OF THE INVENTION

25 Figure 1 is a cross-section of a prior art semiconductor substrate 10 shown at an early fabrication stage for forming a flash memory device 100. As depicted, substrate 10 comprises a core region 10C and a periphery region 10P. The core memory stacks 12, 13 and periphery memory region 9 are provided with an anti-reflective coating 14 having a typical thickness d

in a range of 300Å to 1000Å. Core memory stacks 12, 13, at this stage of fabrication, and as depicted in Figure 1, may comprise a thin layer of silicon dioxide 11, a first polysilicon layer P1, a dielectric layer D1 over layer P1 and a second polysilicon layer P2 over layer D1. The spacing S between stacks 12 and 13 is in the sub-micron range which necessitates the formation of spacers between stacks 12 and 13 to protect the corner regions 11a of the silicon dioxide layers 11 during various etching operations. The peripheral memory region 9 may comprise, as depicted in Figure 1, a layer of polysilicon material P2 for use in formation of the periphery memory elements. Further, as previously discussed, the prior art processes utilize anti-reflective coatings 14 multiple times, in combination with photoresist material R, for use in formation of resist patterns, such as resist patterns 15 and 16.

Figure 2 shows a flash memory device 200, in accordance with the present invention, at a fabrication stage where, rather than applying photoresist material, to form subsequent other resist patterns, the first anti-reflective coating layers 14 are used only to form the core memory stacks 12 and 13 and the peripheral memory region 9. Accordingly, Figure 3 shows the device 200 with anti-reflective coating 14, depicted in Figure 2, stripped from the core memory stacks 12 and 13 and the peripheral memory region 9.

Figure 4 shows the present invention, where, in preparation for subsequent patterning processes, a second coating of anti-reflective coating material 17, such as silicon oxynitride (SiON), silicon nitride (Si₃N₄), and silicon germanium (SiGe), or other suitable material with dual purpose optical properties compatible with other fabrication processes, is deposited in a thickness in a range of 300Å to 1000Å over the core memory stacks 12 and 13, the spacing S between stack 12 and 13, floor region F, the core-periphery interface region CP, and over the periphery memory region 9. As shown in Figure 5, the second coating 17 is used for patterning any remaining gate structures, such periphery gate structures 7 and 8 in the periphery memory region 9, depicted in Figure 4, by appropriate masking and etching operations.

Figure 6 shows the present invention where spacers 18 are defined on the sidewalls of the core memory gate structure 12 and 13 after stripping the second anti-reflective coating 17 from over the second polysilicon layers P2 of core memory gate stacks 12 and 13, and from over the periphery memory gate structures 7 and 8. Accordingly, the present invention

provides a dual gate semiconductor structure 200 whose sidewall spacers 18 of core memory gate structures 12 and 13 are formed by a first and second anti-reflection fabrication process. In accordance with the present invention, the sidewall spacers 18 of the dual transistor gate structure in the core memory region are left coated with the second anti-reflective coating material, such as silicon oxynitride (SiON), silicon nitride (Si₃N₄), and silicon germanium (SiGe), or other material having optical properties compatible with subsequent fabrication processing, to form sidewall spacers for use in subsequent implant and salicidation steps, commonly used during fabrication of the semiconductor device.

Information as herein shown and described in detail is fully capable of attaining the above-described object of the invention, the presently preferred embodiment of the invention, and is, thus, representative of the subject matter which is broadly contemplated by the present invention. The scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and is to be limited, accordingly, by nothing other than the appended claims, wherein reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural and functional equivalents to the elements of the above-described preferred embodiment and additional embodiments that are known to those of ordinary skill in the art are hereby expressly incorporated by reference. And are intended to be encompassed by the present claims. Moreover, no requirement exists for a device or method to address each and every problem sought to be resolved by the present invention, for such to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims. However, it should be readily apparent to those of ordinary skill in the art that various changes and modifications in form, semiconductor material, and fabrication material detail may be made without departing from the spirit and scope of the inventions as set forth in the appended claims. No claim herein is to be construed under the provisions of 35 U.S.C. 112, sixth paragraph, unless the element is expressly recited using the phrase "means for."

CLAIMS

What is Claimed:

1. A semiconductor memory device comprising:
 - a. a silicon substrate;
 - b. a peripheral memory region delineated on said substrate, said peripheral memory region having at least one peripheral memory element formed thereon;
 - c. a core memory region also delineated on said substrate, said core memory region having at least one set of dual gate core memory structures formed thereon, said dual gate core memory structures comprising a stacked layer arrangement of semiconductor and dielectric material defining respective sidewall portions; and
 - d. dual-purpose sidewall spacer structures formed on said respective sidewall portions, said spacer structure being formed from anti-reflective coating material and being used for lithographic patterning and for protecting said stacked layer arrangement during etching operations.
2. A semiconductor memory device, as recited in Claim 1, wherein:

said anti-reflective coating material being selected from an anti-reflective coating material group consisting of silicon oxynitride (SiON), silicon nitride (Si₃N₄), and silicon germanium (SiGe), said material group having anti-reflective optical properties and being compatible with ion implantation and salicidation fabrication processes.
3. A semiconductor memory device, as recited in Claim 2, wherein:

said anti-reflective coating material being deposited in a thickness ranging from 300Å to 1000Å.

4. A semiconductor memory device comprising:
- a. a silicon substrate;
 - b. a peripheral memory region delineated on said substrate, said peripheral memory region having at least one peripheral memory element formed thereon;
 - c. a core memory region also delineated on said substrate, said core memory region having at least one set of dual gate core memory structures formed thereon, said dual gate core memory structures comprising a stacked layer arrangement of semiconductor and dielectric material defining respective sidewall portions; and
 - d. dual-purpose spacer structures formed on said respective sidewall portions, said dual-purpose spacer structures being formed from anti-reflective coating material and being selected from an anti-reflective coating material group consisting of silicon oxynitride (SiON), silicon nitride (Si₃N₄), and silicon germanium (SiGe), said material group having anti-reflective optical properties and being compatible with ion implantation and salicidation fabrication processes.
5. A semiconductor memory device, as recited in Claim 4, wherein:
said anti-reflective coating material being deposited in a thickness ranging from 300Å to 1000Å.
6. A method of fabricating a semiconductor memory device, said method comprising the steps of:
- a. providing a semiconductor substrate;
 - b. fabricating core and periphery memory regions on said substrate
 - c. depositing a first layer of anti-reflective coating material for use in lithographic patterning of said core and periphery memory region;
 - d. patterning and forming at least one pair of dual gate stacked structures on said core memory region, each one of said dual gate stacked structures having

respective sidewalls;

- e. stripping all of said first layer of anti-reflective coating material deposited in said step (c);
- f. depositing a second layer of anti-reflective coating material over the dual gate stacked structures on said core memory region and on said periphery memory region after being stripped in accordance with said step (e), said depositing step including depositing said second layer of anti-reflective coating material on said sidewalls and on floor regions between said gate stacked structure and between a core memory and periphery memory interface region;
- g. patterning and forming any remaining gate structure on said periphery memory regions; and
- h. forming dual-purpose spacer structures on said sidewalls by stripping said second layer of anti-reflective coating material deposited over said floor region, over said interface region, over said dual gate stacked structure and over any formed peripheral gate structure, but not from said sidewalls, said dual-purpose spacer structures being used for lithographic patterning and for protecting said dual gate stacked structure during etching operations.

7. A method of fabricating a semiconductor memory device, as recited in Claim 6, wherein: said step (f) comprises selecting said anti-reflective coating material from an anti-reflective coating material group consisting of silicon oxynitride (SiON), silicon nitride (Si₃N₄), and silicon germanium (SiGe), said material group having anti-reflective optical properties and being compatible with ion implantation and salicidation fabrication processes.

8. A method of fabricating a semiconductor memory device, as recited in Claim 6, wherein said step (h) results in producing a semiconductor memory device, said device comprising:

- a. said semiconductor substrate;
- b. at least one peripheral memory element formed during said step (g); and
- c. at least one set of said dual gate core memory structures having said dual-purpose sidewall spacer structures formed during said step (h).

9. A method of fabricating a semiconductor memory device, as recited in Claim 7, wherein said step (h) results in producing a semiconductor memory device, said device comprising:

- a. said semiconductor substrate;
- b. at least one peripheral memory element formed during said step (g); and
- c. at least one set of said dual gate core memory structures having said dual-purpose sidewall spacer structures formed during said step (h).

10. A method of fabricating a semiconductor memory device, said method comprising the steps of:

- a. providing a semiconductor substrate;
- b. fabricating periphery memory regions on said substrate, said periphery memory region comprising at least one layer of a semiconductor material formed over said substrate;
- c. fabricating core memory regions on said substrate, said core memory regions comprising a layer arrangement of dielectric and semiconductor material;
- d. depositing a first layer of anti-reflective coating material over said layer arrangement and over said periphery memory region;
- e. patterning at least one pair of dual gate stacked structure on said core memory region, each one of said dual gate stacked structure having respective sidewalls;
- f. stripping any first layer of anti-reflective coating material remaining on said dual gate stacked structure and on said periphery memory region;

- g. depositing a second layer of anti-reflective coating material over the dual gate stacked structures on said core memory region and on said periphery memory region after being stripped in accordance with said step (f), said depositing step including depositing said second layer of anti-reflective coating material on said sidewalls and on floor regions between gate stacked structure and between core memory and periphery memory interface regions;
- h. patterning and forming any remaining gate structure on said periphery memory regions; and
- i. forming dual-purpose spacer structures on said sidewalls by stripping said second layer of anti-reflective coating material deposited over said dual gate stacked structure and over any formed peripheral gate structure, but not from said sidewalls, said dual-purpose spacer structures being used for lithographic patterning and for protecting said dual gate stacked structure during etching operations.

11. A method of fabricating a semiconductor memory device, as recited in Claim 10, wherein:

said step (g) comprises selecting said anti-reflective coating material from an anti-reflective coating material group consisting of silicon oxynitride (SiON), silicon nitride (Si₃N₄), and silicon germanium (SiGe), said material group having anti-reflective optical properties and being compatible with ion implantation and salicidation fabrication processes.

12. A method of fabricating a semiconductor memory device, as recited in Claim 10, wherein said step (i) results in producing a semiconductor memory device, said device comprising:

- a. said semiconductor substrate;
- b. at least one peripheral memory gate structure formed during said step (h); and
- c. at least one set of said dual gate core memory structures having said dual-purpose sidewall spacer structures formed during said step (i).

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13. A method of fabricating a semiconductor memory device, as recited in Claim 11, wherein said step (i) results in producing a semiconductor memory device, said device comprising:

- a. said semiconductor substrate;
- b. at least one peripheral memory gate structure formed during said step (h); and
- c. at least one set of said dual gate core memory structures having said dual-purpose sidewall spacer structures formed during said step (i).

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DUAL-PURPOSE ANTI-REFLECTIVE COATING AND SPACER
FOR FLASH MEMORY AND OTHER DUAL GATE TECHNOLOGIES
AND METHOD OF FORMING

ABSTRACT OF THE DISCLOSURE

A dual gate semiconductor device, such as a FLASH memory semiconductor device, whose plurality of dual gate sidewall spacer structure is formed by a first and second anti-reflection fabrication process. The sidewall spacers of the dual transistor gate structures in the core memory region are left coated with the second anti-reflective coating material, after being used for gate patterning, to act as sidewall spacers for use in subsequent ion implant and salicidation fabrication steps. The second anti-reflective coating material is selected from a material group such as silicon oxynitride (SiON), silicon nitride (Si_3N_4), and silicon germanium (SiGe), or other anti-reflective coating material having optical properties and that are compatible with the subsequent implant and salicidation steps.



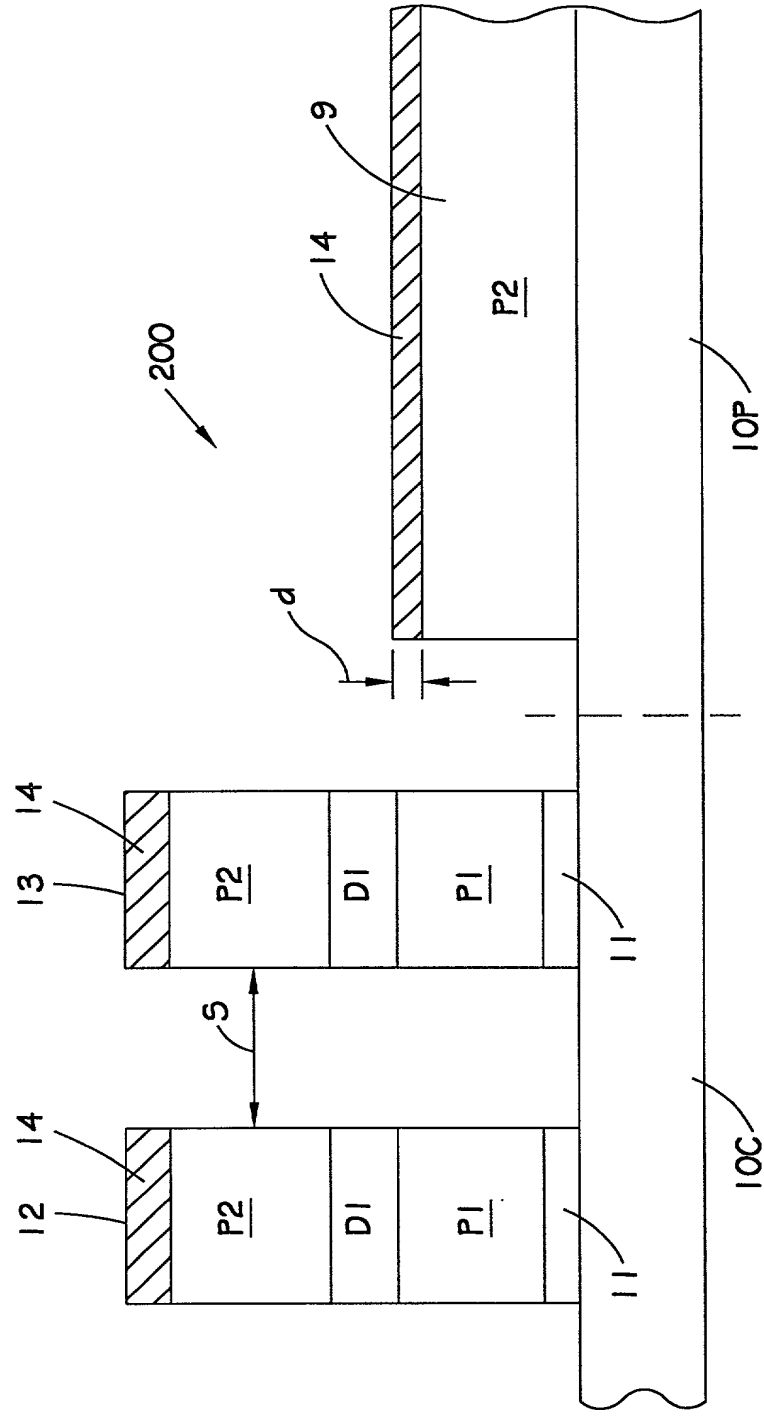


Figure 2.0

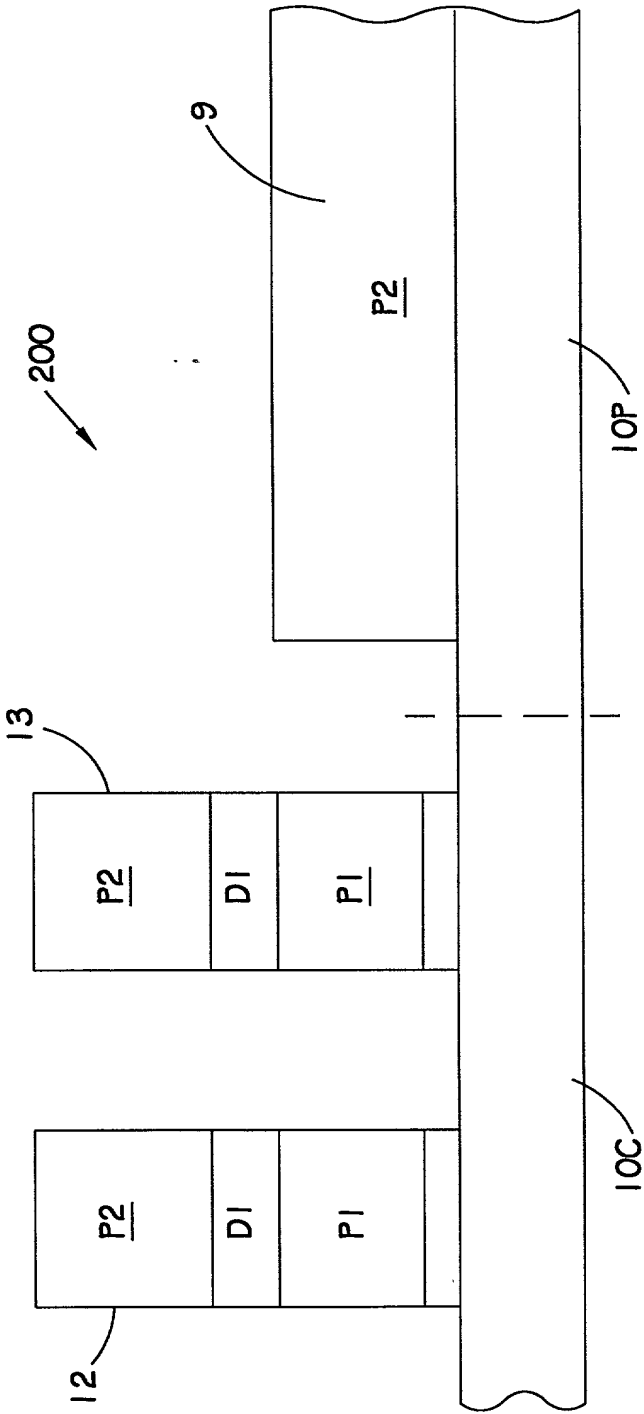


Figure 3.0

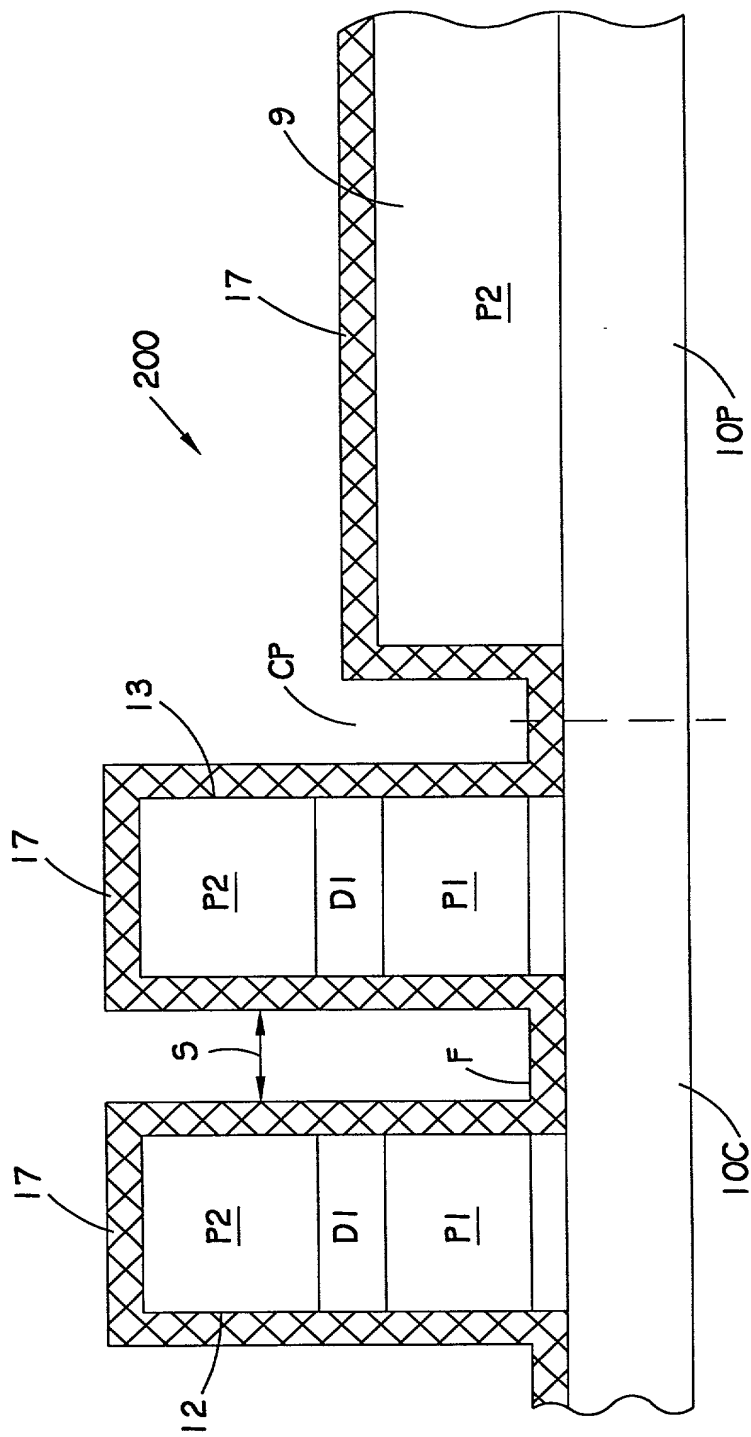


Figure 4.0

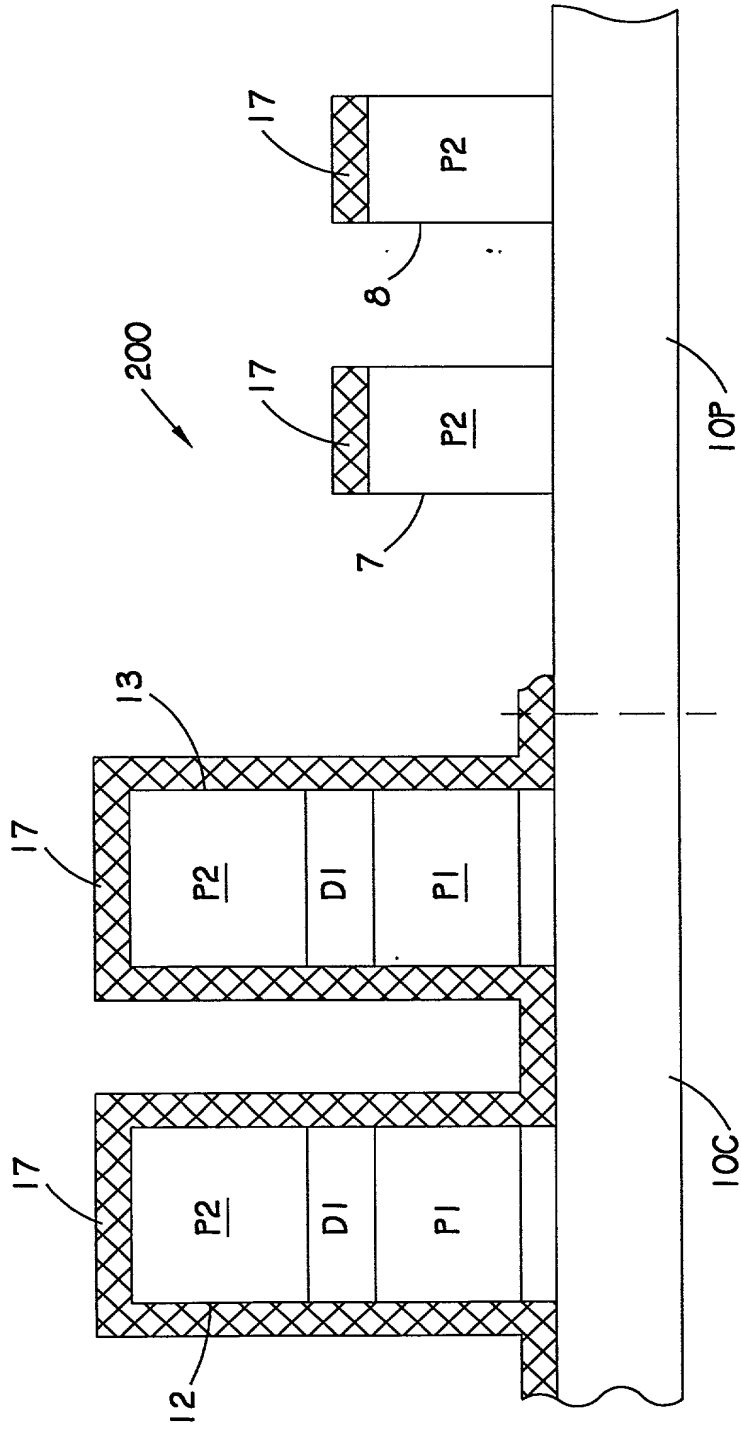


Figure 5.0

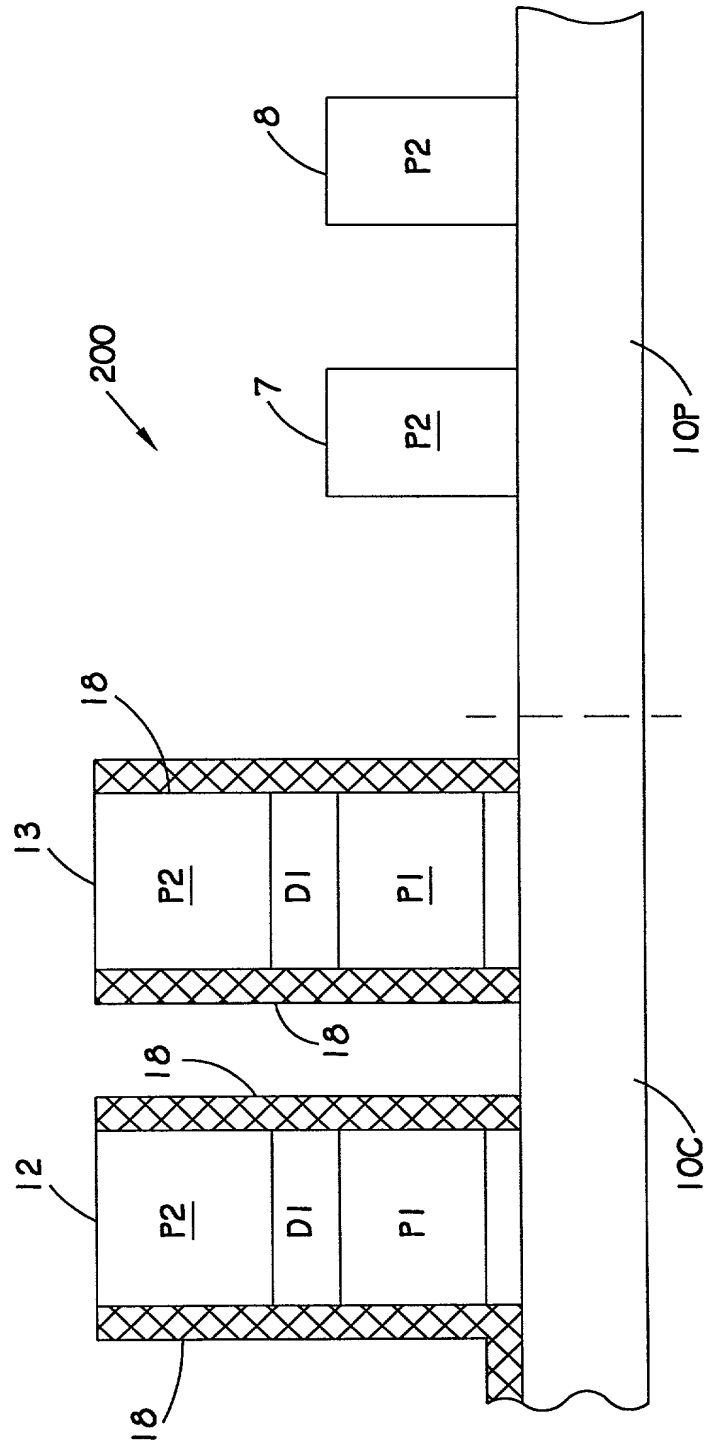


Figure 6.0

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**Declaration and Power of Attorney
for Patent Application**

**ATTORNEY'S DOCKET NO.
P1025**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

DUAL-PURPOSE ANTI-REFLECTIVE COATING AND SPACER FOR FLASH MEMORY AND OTHER
DUAL GATE TECHNOLOGIES AND METHOD OF FORMING

the specification of which ☒ is attached hereto.
☐ was filed on _____
Application Serial No. _____
and was amended on _____

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119, of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s) (Number/Country/Date Filed/Priority Claims: Yes/No)

_____ No _____

I hereby claim the benefit under Title 35, United States Code, Section 120, of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a), which occurred between the filing date of the prior application and the national or PCT international filing date of this application (list application Serial No./Filing Date/Status):

_____ Provisional Application No. 60/159,235: 10/13/99 _____

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Dated: 6/2/00
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